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LIST OF PRIOR ART CITED BY APPLICANT

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Atty. Docket No.	Serial No.
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Applicant	
David M. Fried, et al.	
Filing Date	**Group**
December 14, 2001	Unassigned

U.S. PATENT DOCUMENTS

EXAMINER INITIAL*		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (if appropriate)
	AA	3,872,491	3/18/75	Hanson, et al.			
	AB	5,315,143	5/24/94	Tsuji			
	AC	5,338,959	8/16/94	Kim, et al.			
	AD	5,365,083	11/15/94	Tada			
	AE	5,391,506	2/21/95	Tada, et al.			
	AF	6,031,269	2/29/00	Liu			
	AG	6,069,390	5/30/00	Hsu, et al.			
	AH	6,150,687	11/21/00	Noble, et al.			
	AI	6,207,530 B1	3/27/01	Hsu, et al.			
	AJ	6,207,985 B1	3/27/01	Walker			
	AK	6,242,783	6/5/01	Ohmi, et al.			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

		Leland Chang, et al., "Gate Length Scaling and Threshold Voltage Control of Double-Gate MOSFET's", Department of Electrical Engineering and Computer Sciences, University of California, 2000 IEEE.
		Keunwoo Kim, et al., "Optimal Double-Gate MOSFET's : Symmetrical or Asymmetrical Gates?, 1999 IEEE International SOI Conference, Oct. 1999, (pp.98-99).
		Yan, et al., "Scaling the Si MOSFET : From Bulk to SOI Bulk, IEEE Transactions on Electron Devices, Vol. 39, No. 7, p. 1704, July 1992.

EXAMINER	DATE CONSIDERED
	11/23/03

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.